

ABSTRACT OF THE DISCLOSURE

An embodiment of the invention provides a circuit and method for improving noise tolerance in multi-threaded memory circuits. A PFET is added to the receiving input of each memory cell. The gate of the PFET is connected to the output of the
5 memory cell and the source of the PFET is connected to the control signal of the memory cell. In the case where the dataline is charged near ground and a memory cell, with a high value, is read, and the control signal is high, noise tolerance is improved by the addition of the PFET to the memory cell. The invention does not introduce additional drive fights during writes, when the control signal is low.